

COURSE DESCRIPTION

NAME OF INSTITUTION	Lahore Garrison University
PROGRAM (S) TO BE EVALUATED	Computer Science , Spring 2022

Course Description :

Course Code	CSC332																		
Course Title	Digital Logic Design																		
Credit Hours	3+1																		
Prerequisites by Course(s) and Topics	Applied Physics																		
Assessment Instruments with Weights (homework, quizzes, midterms, final, programming assignments, lab work, etc.)	SESSIONAL (Quizzes, Assignments, Presentations) =25 % Midterm Exam =25 % Final Exam = 50%																		
Course Coordinator	Huma Chaudhry																		
URL (if any)																			
Current Catalog Description	Digital fundamentals Floyd (11th edition)																		
Textbook (or Laboratory Manual for Laboratory Courses)	Digital fundamentals Floyd (11th edition)																		
Reference Material	• Fundamentals of Digital Logic with Verilog Design, Stephen Brown, 2/e • Logic and Computer Design Fundamentals by M. Mano 2nd edition Publisher Prentice Hall																		
Course Goals	The Goals of the course is: CLO1: Acquire knowledge related to the concepts, tools, and techniques for the design of digital electronic circuits CLO2: Demonstrate the skills to design and analyze both combinational and sequential circuits using a variety of techniques 3. Apply the CLO3: Apply the acquired knowledge to simulate and implement small-scale digital circuits																		
Course Learning Outcomes (CLOs):	<table><tr><td>At the end of the course the students will be able to:</td><td>Domain</td><td>BT Level*</td></tr><tr><td>CLO1: Acquire knowledge related to the concepts, tools, and techniques for the design of digital electronic circuits</td><td></td><td></td></tr><tr><td>CLO2: Demonstrate the skills to design and analyze both combinational and sequential circuits using a variety of techniques 3.</td><td></td><td></td></tr><tr><td>CLO3: Apply the acquired knowledge to simulate and implement small-scale digital circuits</td><td></td><td></td></tr><tr><td>CLO4: Understand the relationship between abstract logic characterizations and practical electrical implementations.</td><td></td><td></td></tr><tr><td>* BT= Bloom's Taxonomy, C=Cognitive domain, P=Psychomotor domain, A= Affective domain</td><td></td><td></td></tr></table>	At the end of the course the students will be able to:	Domain	BT Level*	CLO1: Acquire knowledge related to the concepts, tools, and techniques for the design of digital electronic circuits			CLO2: Demonstrate the skills to design and analyze both combinational and sequential circuits using a variety of techniques 3.			CLO3: Apply the acquired knowledge to simulate and implement small-scale digital circuits			CLO4: Understand the relationship between abstract logic characterizations and practical electrical implementations.			* BT= Bloom's Taxonomy, C=Cognitive domain, P=Psychomotor domain, A= Affective domain		
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Topics Covered in the Course, with Number of Lectures on Each Topic (assume 15-week instruction and one-hour lectures)	Week	Lecture	Topics Covered
	Week 1	1	Introduction, Binary Numbers,
		2	Number Conversion, Decimal Numbers
	Week 2	3	1's and 2's Complements, Arithmetic Operations with unsigned numbers
		4	Arithmetic Operations with signed numbers
	Week 3	5	Octal & Hexadecimal number
		6	Conversions, Binary Coded Decimal (BCD)
	Week 4	7	The Inverter, AND, OR gates
		8	NOR and NAND XOR and XNOR gates
	Week 5	9	Boolean Algebra Rules, DeMorgan's Theorem
		10	Simplification using Boolean algebra
	Week 6	11	Karnaugh Map, SOP and POS expressions, standardization of logic expressions
		12	Karnaugh Map, SOP, POS minimization 3 variable k-maps and 4 variable k-maps
	Week 7	13	5-variable k-maps and simplification of logic circuits using k-maps
		14	Basic Combinational logic circuits Designing of Combinational logic circuits
	Week 8	1 hours	Mid Term
	Week 9	15	Universal property of NAND gates and NOR gates
		16	Combinational logic using NOR gates, Combinational logic using NOR gates
	Week 10	17	Basic Adders, Half Adders Full Adders
		18	Parallel Binary Adders, Basic Subtractors
	Week 11	19	Logic Comparators and Logic Multipliers
		20	Decoders
	Week 12	21	Encoder
		22	Multiplexer or Data selector
	Week 13	23	De-Multiplexer, Application of MUX and DeMUX
		24	Latches
	Week 14	25	Gated Latches, Edge-Triggered Flip Flops
		26	Edge-Triggered Flip Flops D-Flip flop
	Week 15	27	S-R Flip Flops, J- K Flip Flops
		28	SISO shift registers, SIPO shift registers PIPO shift registers.
	Week 16	29	Synchronous/Asynchronous counter operation
		30	Real-time logic and arithmetic circuits implementation, Programmable Logic Devices
	Week 17	2 hours	Final Term
Laboratory Projects/Experiments Done in the Course			
Programming Assignments Done in the Course			

Instructor Name	Huma Chaudhry
Instructor Signature	
Date	